| Q.P. Code:16CS506 | | | |
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| Reg. | No: | | |
| SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR (AUTONOMOUS) B.Tech II Year I Semester (R16) Regular Examinations November 2017 DIGITAL LOGIC DESIGN (Computer Science & Engineering) | | | |
| Time: 3 hours Max Marks: 60 | | | |
| | nou | (Answer all Five Units 5 X 12 = 60 Marks) | |
| UNIT-I | | | |
| 1 | а | Convert the following i) $(1AD)_{16}=()_{10}$ ii) $(453)_8=()_{10}$ iii) $(10110011)_2=()_{10}$ iv) $(5436)_{10}=()_{16}$ | 4M |
| | b | Explain the basic properties of Boolean algebra. | 8M |
| | | OR | |
| 2 | а | Explain about complements with examples? | 8M |
| | b | Prove that $ABC + ABC' + AB'C + A'BC = AB + AC + BC$ | 4M |
| 3 | | UNIT-II Simplify the Boolean expression $f(A,B,C,D,E) = \sum m (0,3,4,7,8,12,14,16,19,20,23,24,26,28)$ | 12M |
| | | OR | |
| 4 | | Explain NAND- NOR implementations? | 12M |
| | | UNIT-III | |
| 5 | | Design a combinational circuit which accepts 3 bit binary number and converts its equivalent Excess 3 code | 12M |
| | | OR | |
| 6 | a b | Define Multiplexer. Explain in details about the functionality of 8 to 1 Multiplexer. Design and Explain the operation of Full Adder. | 6M 6M |
| 7 | 0 | Explain the operation of SP flip flop using NOP and NAND gate 2 | <i>C</i> M |
| 7 | a b | Design and draw the 3 bit up-down synchronous counter? | 6M |
| | | OR | |
| 8 | а | Draw and explain the operation of T Flip-Flop? | 6M |
| | b | Explain the operation of Ring counter | 6M |
| 9 | | Design a Combinational Circuit using PAL by considering the following Boolean functions given in sum of minterms: w(A = B = C = D) = 2(2 - 12 - 13) | |
| | | | 12M |
| 10 | | Explain about Error Detecting and Error correcting codes with example? | 12M |
| | | *** END *** | |